In the Claims:

No amendments have been made to the listing of claims.

1. (*Previously Presented*) A circuit arrangement, comprising: (a) a plurality of hardware resources, wherein each hardware resource has a power mode configurable between at least first and second power consumption states; and (b) a processor coupled to the plurality of hardware resources, the processor configured to process program code that includes at least one power control instruction that includes an operand having power control information disposed therein, wherein the processor is configured to process the power control instruction by selectively setting power modes of at least two hardware resources among the plurality of hardware resources based upon the power control information disposed in the power control instruction, and wherein the processor is further configured to maintain the power modes of the at least two hardware resources to that specified in the power control instruction while processing at least one subsequent instruction in the program code.

2. (*Previously Presented*) The circuit arrangement of claim 1, wherein the power control instruction includes an opcode that uniquely identifies the power control instruction.

3. (*Previously Presented*) The circuit arrangement of claim 1, further comprising: (a) a support register that stores power modes state information for the plurality of hardware resources; and (b) enabling logic coupled to the support register and configured to control the power modes of the plurality of hardware resources responsive to the power modes state information stored in the support register, wherein the processor is configured to selectively set the power modes of the at least two hardware resources by storing the power control information from the power control instruction in the support register.

4. (*Previously Presented*) The circuit arrangement of claim 3, wherein the support register comprises a power modes register.

5. (*Original*) The circuit arrangement of claim 3, wherein the support register includes additional status information that is unrelated to power dissipation control.

6. (*Previously Presented*) The circuit arrangement of claim 3, wherein a subset of the plurality of hardware resources comprises a plurality of banks of registers defining a register file, wherein the enable logic includes a plurality of enable circuits, each associated with a bank of registers from the plurality of banks of registers, and each configured to selectively disable its associated bank of registers responsive to an enable signal, wherein the enable logic is further configured to generate the enable signal for each bank of registers from the power modes state information stored in the support register.

7. (*Previously Presented*) The circuit arrangement of claim 6, wherein each bank of registers includes at least one clock input, address input and data input, and wherein the enable circuit for each bank of registers is configured to selectively gate off the clock, address and data inputs for its associated bank of registers in response to the enable signal provided thereto.

8. (*Previously Presented*) The circuit arrangement of claim 1, wherein each hardware resource is selected from the group consisting of a register file, a register bank, a register, a cache, a bus interface unit, a bus, a functional unit, a functional block and an instruction decoder.

9. (*Original*) The circuit arrangement of claim 1, wherein the processor is configured to process explicitly parallel instructions, and wherein the power control instruction comprises an operation among a plurality of operations in an explicitly parallel instruction.

10. (*Original*) The circuit arrangement of claim 9, wherein the processor is selected from the group consisting of a VLIW processor and an EPIC processor.

11. (*Original*) The circuit arrangement of claim 1, wherein the processor comprises a superscalar processor.

12. (*Original*) The circuit arrangement of claim 1, wherein the processor is configured to assign a side effect to the power control instruction to limit run-time speculation thereof.

13. (*Original*) The circuit arrangement of claim 1, wherein the power control information in the operand identifies a register within which power modes state information for the at least two hardware resources is stored, and wherein the processor is configured to selectively set the power modes of the at least two hardware resources by retrieving the power modes state information from the register identified by the power control information in the operand.

14. (*Original*) The circuit arrangement of claim 1, wherein the plurality of hardware resources are disposed in the processor.

15. (*Original*) The circuit arrangement of claim 1, wherein at least one hardware resource is disposed outside of the processor but on the same integrated circuit as the processor.

16. (*Original*) The circuit arrangement of claim 1, wherein at least one hardware resource is disposed on a separate integrated circuit from the processor.

17. (*Original*) An integrated circuit comprising the circuit arrangement of claim 1.

18. (*Previously Presented*) A program product comprising a hardware definition program defining the circuit arrangement of claim 1, and a signal-bearing tangible medium bearing the hardware definition program, wherein the signal-bearing tangible medium includes at least one of a transmission medium and a recordable medium.

19. (*Previously Presented*) A method of executing program code on a processor coupled to a plurality of hardware resources, each having a power mode configurable between at least first and second power consumption states, the method comprising: (a) processing a power control instruction from the program code by selectively setting power modes of at least two hardware resources among the plurality of hardware resources based upon power control information disposed in an operand of the power control instruction; and (b) processing at least one subsequent instruction in the program code while the power modes of the at least two hardware resources are set to that specified by the power control information of the power control instruction.

20. (*Original*) The method of claim 19, wherein the power control instruction further includes an opcode that uniquely identifies the power control instruction.

21. (*Original*) The method of claim 19, wherein the processor includes a support register that is utilized by enable logic in the processor to set the power modes of the plurality of hardware resources, and wherein selectively setting the power modes of at least two hardware resources includes storing the power control information in the support register.

22. (*Original*) The method of claim 21, further comprising, after processing the first subsequent instruction, processing a second power control instruction from the program code by storing second power control information disposed in an operand thereof in the support register such that the power mode of a first hardware resource is modified, and processing a second subsequent instruction after processing the second power control instruction, whereby the second subsequent instruction is processed while the power mode of the first hardware resource is set to that specified in the second power control instruction.

23. (*Original*) The method of claim 21, wherein a subset of the plurality of hardware resources comprises a plurality of banks of registers defining a register file, wherein the enable logic includes a plurality of enable circuits, each associated with a bank of registers from the plurality of banks of registers, and each configured to selectively disable its associated bank of registers responsive to an enable signal, the method further comprising generating the enable signal for each bank of registers from the power modes state information stored in the support register.

24. (*Original*) The method of claim 23, wherein each bank of registers includes at least one clock input, address input and data input, and wherein the enable circuit for each bank of registers is configured to selectively gate off the clock, address and data inputs for its associated bank of registers in response to the enable signal provided thereto.

25. (*Original*) The method of claim 19, wherein each hardware resource is selected from the group consisting of a register file, a register bank, a register, a cache, a bus interface unit, a bus, a functional unit, a functional block and an instruction decoder.

26. (*Original*) The method of claim 19, wherein the processor is configured to process explicitly parallel instructions, and wherein the power control instruction comprises an operation among a plurality of operations in an explicitly parallel instruction.

27. (*Previously Presented*) A method of generating program code for execution by a processor coupled to a plurality of hardware resources, each having a power mode configurable between at least first and second power consumption states, the method comprising: (a) analyzing at least a portion of a program to determine utilization of the plurality of hardware resources by the processor during execution of at least a section of program code from the program; (b) based upon the determined utilization of the plurality of hardware resources, inserting a power control instruction into the program, the power control instruction including power control information disposed in an operand

thereof that specifies power modes for at least two hardware resources among the plurality of hardware resources, wherein the power control instruction is configured to be executed prior to at least one non-power control instruction in the program code, and wherein the program code is configured to cause the processor to dynamically set the power modes for the at least two hardware resources to that specified in the power control instruction such that the non-power control instruction will be processed while the power modes of the at least two hardware resources are maintained at that specified in the power control instruction.

28. (*Original*) The method of claim 27, wherein analyzing the program and inserting the power control instruction are performed during at least one of compilation and optimization of the program.

29. (*Original*) The method of claim 27, wherein analyzing the program and inserting the power control instruction are performed concurrently with execution of the program by the processor.

30. (*Original*) The method of claim 27, further comprising consolidating resource usage in the program to a limited subset of hardware resources prior to inserting the power control instruction into the program.